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Comparative Study of the Device Parameters of Schottky Barrier Solar Cells and Homo-Heterojunction Solar Cells

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Abstract

This paper reports how the p – CdTe layers grown on Schottky heterostructure influences the opto-electronic behaviour of homo-heterojunction solar cell devices fabricated from CdTe – based device architecture. Two sets of device architecture namely n – n Schottky barrier solar cells and homo-heterojunction – based solar cells with n – n – p device structure was investigated. Schottky barrier solar cells were fabricated using glass/FTO/n – CdS/n – CdTe/Au device structure and this serves as the baseline for comparison with the homo-heterojunction solar cells having p – CdTe layers. The multijunction-based homo-heterojunction solar cells with the n – n – p device architecture was fabricated using glass/FTO/n – CdS/n – CdTe/p – CdTe/Au. The p – CdTe layers grown on n – CdTe affect the solar cell and diode current – voltage characteristics, hence influencing the device electronic parameters. Non – linear and rectifying responses were observed for homo-heterojunction solar cells and n – n Schottky barrier solar cells respectively, when measured under dark condition. Under illumination condition, the cell parameters of the homo-heterojunction solar cells improved as compared to the Schottky barrier solar cells. Short circuit current density values of 27.0 $mAcm^{-2}$ and 38.0 $mAcm^{-2}$ were obtained for the Schottky barrier and homo-heterojunction – based solar cells respectively. Overall, higher efficiency values of ~4.91% and 7.39% were obtained for the Schottky barrier and homo-heterojunction – based solar cells respectively. Some of the electronic parameters influenced by the insertion of p – CdTe layers on the Schottky heterostructure are: leakage currents, potential barrier heights, ideality factor, series resistance and shunt resistance; the detailed results of these electronic parameters are presented in this article.

Keywords: n – n – p Homo-heterojunction Solar Cells, n – n Schottky Barrier Solar Cells, Non – linear Response, Rectifying Response, Efficiency.

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Introduction

The inadequate exploitation of solar energy has contributed to insufficient energy supply in developing countries such as Nigeria. Solar energy materials mainly semiconductors have been utilised by researchers in the production of alternative renewable energy. These semiconductors have been classified as elemental and compound-based semiconductor materials. Silicon which serves as the major constituent of the first-generation solar cell is an inorganic material which belongs to the elemental-based semiconductor and the cost of production of solar cells from silicon material is actually on the high side due to the numerous and complex production processes involved (Green, 2022).

The reports published by (Green et al., 2024) revealed that at the laboratory scale level, monocrystalline Si solar cells have efficiencies of (26.8±0.4)%. The huge manufacturing cost of first-generation solar cells makes their dollars per Watt to be on the high side (Kant & Singh, 2022). Due to the high cost involved, researchers have paid attention on affordable and efficient

renewable solar sources and production technique which will greatly reduce the solar cell's cost of production and enhance efficiency. The quest to provide affordable, more efficient and renewable solar energy sources with excellent functionality in energy generation has triggered the research into thin film inorganic – based compound semiconductors. The thin film – based solar cells offer advantages of reduced cost, less materials usage and a progressively increasing power conversion efficiency (PCE) (Dharmadasa, 2013; Suthar et al., 2022).

The use of chalcogenides has been widely employed as active layers in thin film photovoltaic due to their high absorption coefficient values and energy band gaps ranging between 1.00 and 3.86 eV (Madugu et al., 2016; Saha et al., 2020). Among these chalcogenides is cadmium telluride (CdTe) which falls within the category of group II-VI compound semiconductors. CdTe is a direct band gap material with high absorption coefficient and energy band gap ranging between ~1.44 and 1.52 eV (Abdul-Manaf et al., 2015; Olusola et al., 2017). CdTe possesses good optoelectronic properties which make it applicable as photovoltaics and radiation detectors. The inherent ability of CdTe to possess p, i, and n-type electrical conduction also makes it viable for applications as homo-junction, hetero-junction and homo-heterojunction – based solar cells (Ali et al., 2020; Dharmadasa, 2014).

Among numerous growth techniques, electrodeposition has been reported as a well – established deposition technique in growing CdTe thin films. The development of the solar cell materials from CdTe – based compound, using a low-cost electrodeposition production process is facile and reproducible making its availability unique and adequate for mass production. The CdTe – based solar cells are inorganic-based devices which belong to the category of second-generation solar cells. The costs of making these second-generation solar cells are low when compared to the first-generation solar cells; the low-cost is a key benefit since smaller amount of materials and reduced production cost are involved in the entire processes.

Currently, the First Solar Company in the United States has accomplished the highest efficiency of (21.0±0.4)% in CdTe thin films at laboratory scale level (Green et al., 2024). However, CdTe have their limitations with respect to the cells maximum output power. Low efficiencies are observed in second-generation solar cell when compared to first-generation silicon solar cell. These limitations observed in CdTe-based solar devices have been addressed by researchers by surface treatment using the right chemical combinations, and annealing to remove defects which have the capability to lower the cell efficiency (Dharmadasa et al., 2017; Olusola et al., 2017). This research uses the approach of developing homo – heterojunction device architecture from chemically treated / annealed layers to create more charge carriers which can improve the cell efficiency. The developed device has the structure glass/FTO/n-CdS/n-CdTe/p-CdTe/Au. The results obtained from the homo – heterostructure was compared with the Schottky barrier device architecture (glass/FTO/n-CdS/n-CdTe/Au) and the results are presented in this article.

2. Methodology

Semiconductors namely: n-type CdS, n-type CdTe, and p-type CdTe used in this work, were synthesised using low-cost electrodeposition technique. Relevant literatures have reported the optimised parameters used in carrying out the thin films deposition (Ojo et al., 2017). The Schottky barrier solar cells (SBSC) were fabricated using the structure glass/FTO/n-CdS/n-CdTe/Au, while the homo-heterojunction solar cells (HHSC) were fabricated using the device structure glass/FTO/n-CdS/n-CdTe/p-CdTe/Au. The electronic properties of the Schottky-based and homo-heterojunction solar cell devices were measured by employing a computerised Keithley2401 source meter instrument (Keithley Instruments Inc., OH, USA).

3. Results and Discussion

A breakdown of the homo heterostructure consists of Schottky heterostructure and p-n homostructure. Schottky barrier type of solar cell based on n-CdTe thin films was formed using glass/FTO/n-CdS/n-CdTe/Au, while homo-heterojunction based type of solar cell was formed using glass/FTO/n-CdS/n-CdTe/p-CdTe/Au. Combining the Schottky heterostructure with the p-CdTe layer of ~120 nm thickness to form a homo heterostructure is essential for further investigation so as to explore the effect of p-type CdTe thin films on the solar cell efficiency.

3.1 n – n Schottky Barrier Solar Cells

Figure 1 shows the I – V (linear – linear curve) characteristics of Schottky barrier solar cells (SBSC) measured under dark condition, while Figure 2 illustrates the log linear I – V curve of the SBSC. Figure 1 shows that the SBSC behaved as a good rectifying diode when measured under dark condition with a threshold voltage (V_t) of ~0.3 V and breakdown voltage (V_{bd}) of ~0.5 V. However, the Schottky diode has high series resistance (R_s) and large shunt resistance (R_{sh}) of ~9.0 kΩ and 0.45 MΩ respectively. The R_s was estimated from the upper forward portion of Figure 1, while R_{sh} was gotten from the distant end of the reverse portion of Figure 1. The large R_{sh} is an advantage in solar cells fabrications because it prevents the creation of alternative paths that photogenerated current can flow, thereby making the bulk of the photogenerated charge carriers to flow through the solar cell rather than the created alternative path. Nonetheless, this effect was not obviously felt in the cell efficiency when measured under illumination due to the extreme R_s value of ~9.0 kΩ obtained from the SBSC when measured under dark condition.

SBSC are known for their high contact resistance most especially, when an interface is created between the semiconductor and metal (Li et al., 2008), The creation of high contact resistance introduces additional resistance to the material which further increases the R_s value in SBSC (Rohatgi et al., 1991). The ideality factor (n) estimated from the gradient of log linear I – V curve illustrated in Figure

2, is useful in indicating the amount of defect levels in the material and the kind of current transport that takes place in a device structure. With *n* value larger than 3.00, there are large defects in the device structure which can trap photogenerated charge carriers. The presence of large R_s in the SBSC and electrons tunneling through the device are possible factors that can boost the *n* value (Echendu & Dharmadasa, 2015).

Figure 2 was used in finding the rectification factor (RF), potential barrier height (ϕ_b), ideality factor (*n*), reverse saturation current (I_s). Figure 2 was plotted from the simplified log linear I – V characteristic of a photovoltaic (PV) device under dark condition and this is described by Eqn. (1) (Dharmadasa, 2013; Sze & Ng, 2007).

$$I_D = I_s . exp\left(\frac{qV}{nkT}\right) \quad (1)$$

where I_D is the forward current measured in dark, I_s is the leakage or reverse saturation current gotten from the extrapolation of the intercept of Log I axis at V = 0, *V* is the forward bias voltage, *n* is the ideality factor, *k* is the Boltzmann constant (1.38×10^{-23} JK^{-1}), T is the room temperature (300 K), *q* is the electronic charge (1.6×10^{-19} C).

The ideality factor, *n* is determined from the gradient, *G* of Eqn. (1). The gradient is given as:

$$G = \frac{q}{2.303 \times nkT} \quad (2)$$

Under dark condition, the SBSC behaves as a Schottky diode with a rectification factor of $10^{1.48}$; this value corresponds to ~30.20. The RF was estimated by the ratio of forward current (I_f) to reverse current (I_r) at a specified bias voltage of 1.0 V. The I_f and I_r values were estimated from the log linear I – V curve as $10^{-4.37}$ and $10^{-5.85}$ respectively.

I_s was determined from the intercept of the log-linear I-V curve, and is a factor which determines the ϕ_b formed at the interface of device structure. The I_s and ϕ_b of the SBSC were estimated to be 19.95 nA and 0.729 eV respectively. Both ϕ_b and I_s are related according to Eqn. (3).

$$\phi_b = \frac{kT}{q} ln\left(\frac{SA^*T^2}{I_s}\right) \quad (3)$$

where *S* is the cell area, and A^* is the Richardson constant (12.0 $Acm^{-2}K^{-2}$) for CdTe thin films.

For a semiconductor with effective mass (m^*), the Richardson constant is given by Eqn. (4) (Rhoderick, 1982).

$$A^* = \frac{4\pi m^* k^2 q}{h^3} \quad (4)$$

where *h* is the Planck's constant (6.626×10^{-30} cm^2kgs^{-1}), m^* is the effective mass of charge carriers and this varies from one material to the other. $m_*^e = 0.1\ m_o$ is the effective electron mass of CdTe, m_o is the rest mass of electron (9.1×10^{-31} kg) (Pugh et al., 1993).

Figure 3 shows the J – V characteristics of SBSC measured under illumination. The series resistance reduced from ~9.0 kΩ under dark condition to ~2.6 kΩ under light condition. The reduction in R_s value ascertain the photoconductivity behaviour of SBSC measured under illumination condition. However, the SBSC still possesses high R_s value under illumination which contributes to the decreased efficiency of the SBSC. The circled section of Figure 3 in the forward bias voltage region further illustrates the high R_s sector of the solar cell.

The parameters which determine the efficiency of solar cells are: open circuit voltage (V_{oc}), short circuit current density (J_{sc}), and fill factor (FF). The V_{oc}, J_{sc}, and FF obtained for the SBSC in Figure 3 are 520 mV, 27 $mAcm^{-2}$, and 0.35 respectively. These values give a solar cell efficiency of ~4.91%.

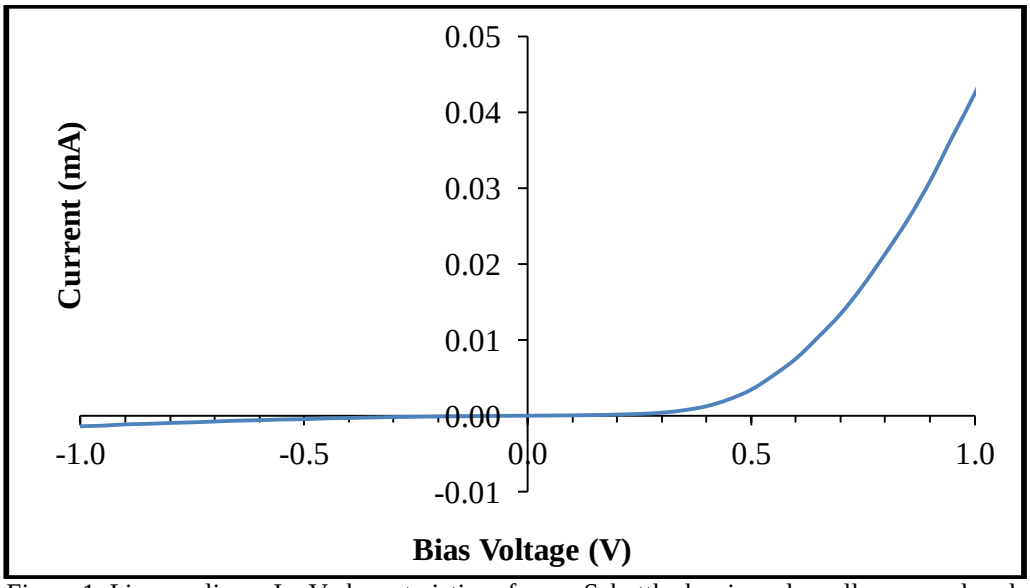

Figure 1: Linear – linear I – V characteristics of n – n Schottky barrier solar cell measured under dark condition.

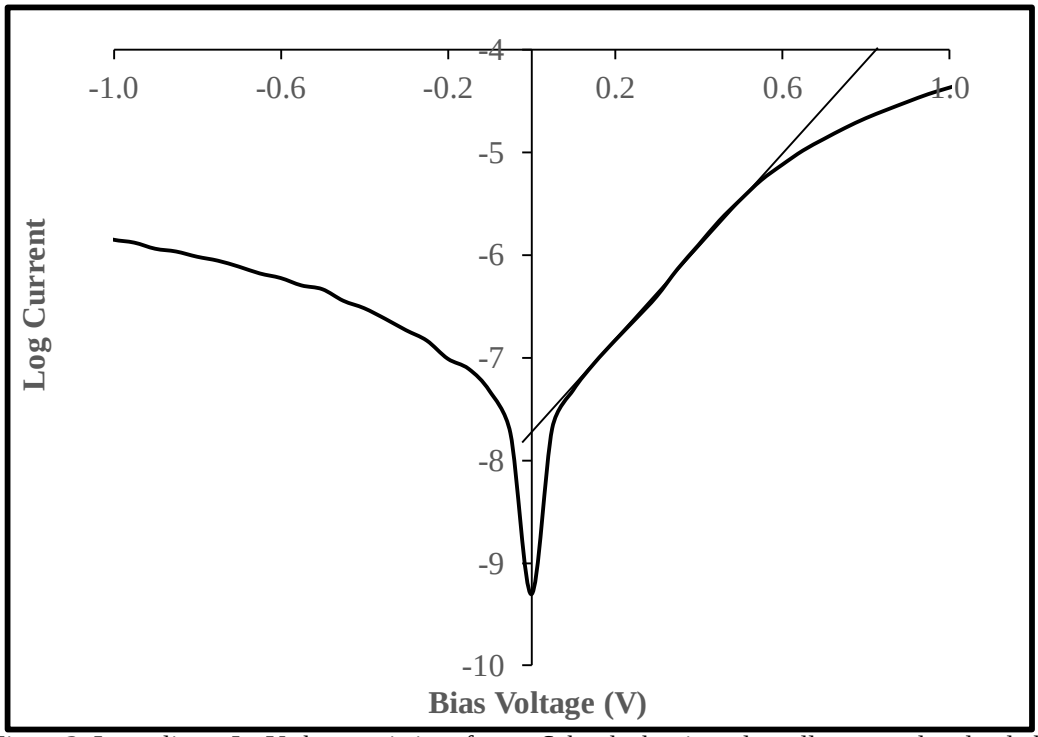

Figure 2: Log – linear I – V characteristics of n – n Schottky barrier solar cell measured under dark condition.

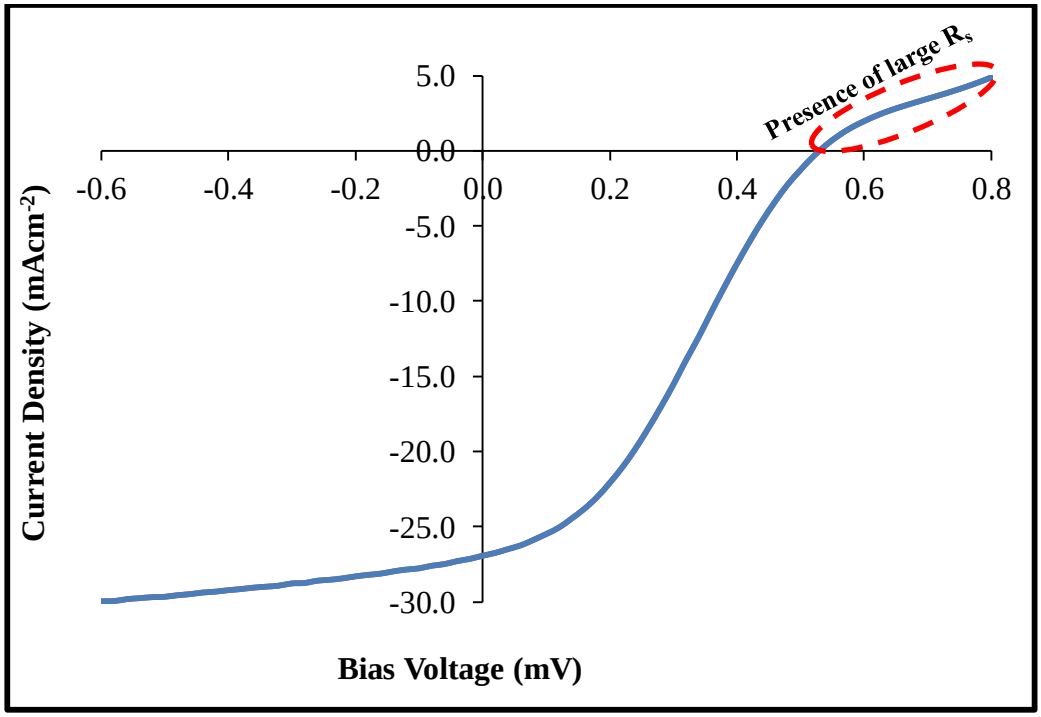

Figure 3: J – V characteristics of n – n Schottky barrier solar cell measured under illumination condition.

3.2 n – n – p Homo – heterojunction Solar Cells

The I – V curves for the n – n – p homo – heterojunction solar cells (HHSC) are given in Figures 4 to 6. Researchers have reported that, the inclusion of a thin film layer of p-type semiconductor on heterostructure semiconducting materials before metal coating can aid the reduction of R_s and enhancement of open circuit voltage (Jones et al., 2009; Sze & Ng, 2007). As explained by Woodcock et al., (1991), the resistance introduced by the back metal contact in SBSC can be minimised by ensuring a higher proportion of tellurium content over the cadmium content on top of the CdTe surface before the metal evaporation. Since R_s are also influenced by the resistance of the back metal contact, lowering the contact resistance will automatically reduce the R_s value (Rohatgi et al., 1991) since Schottky contacts are known to have high R_s value.

An alternative approach to achieve the description given by Woodcock et al., (1991) is to grow a thin film of tellurium rich p-type CdTe on a n – n Schottky barrier solar cell. The inclusion of the p-type layer is expected to reduce the resistance that

should have risen as a result of the Schottky contact. The deposition of p-type CdTe on n – n SBSC structure is also a possible way of bringing the Fermi level close to the valence band. This is expected to produce higher ϕ_b and V_{oc} provided the Te-rich defects associated with p-CdTe are minimised (Dharmadasa et al., 2005). The V_{oc} is dependent on ϕ_b which is a function of the Fermi level pinning location. However, the ϕ_b can be underestimated if there are huge defects in the device.

Figure 4 shows the linear – linear I – V characteristics of n – n – p HHSC, while Figure 5 illustrates the log – linear I – V characteristics of n – n – p HHSC. As seen in Figure 4, the HHSC displays a non – linear response which is an indication of the device poor rectification when measured under dark condition. This implies that the HHSC reported in this work cannot effectively function as a good diode under dark condition. The poor rectifying / non ohmic response of the HHSC makes the RF to be poor, resulting to RF value of $10^{0.02}$ (~1.05), and V_t value of 0.0 V. The non – linear response is a possible indication of the Fermi level pinning before the back-metal contact evaporation. This pinning may be due to presence of surface states at the semiconductor caused by tellurium related defects (Dharmadasa, 1998; Dharmadasa et al., 2005; Lee et al., 1987).

Under an ideal situation, Fermi level should pin to a particular energy level within the material bandgap after back metal contact evaporation; however, there are possibilities for the Fermi level to be pinned before the contact evaporation by the defects present in the device structure. The effect of the defects can be seen in the large *n* value of 3.85. It should be noted that the existence of large *n* value can lead to underestimation of the potential barrier heights of the n – n – p HHSC device structure as seen in this work.

The ideality factor was determined from the slope of the log I – V curve of Figure 5. This type of device is known to possess low R_{sh} and large I_s. As seen in Table 1, HHSC has higher I_s value than SBSC; the leakage current in SBSC is lower, in the range of nanoampere (19.95 nA) unlike the HHSC which is in the range of microampere (39.81 µA). This discrepancy is caused by the higher R_{sh} of the order of MΩ in SBSC and lower R_{sh} of the order of kΩ in the HHSC. Under dark condition, the HHSC exhibits lesser R_s value of ~1.4 kΩ as compared to ~9.0 kΩ observed in the SBSC. The reduction in R_s confirms the previous report by Woodcock et al., (1991), that the incorporation of p-type CdTe on n-type material lowers the R_s value.

Figure 6 shows the J – V characteristics of HHSC measured under illumination. As expected, the R_s reduced from ~1.4 kΩ under dark condition to ~371 Ω under light condition. The reduction in R_s value further confirm the photoconductivity nature of HHSC measured under illumination condition. The low R_s possessed by the HHSC under illumination contributes to the improved efficiency of the HHSC. The circled section of Figure 6 in the forward bias voltage region illustrates the low R_s segment of the solar cell. The V_{oc}, J_{sc}, and FF obtained for the HHSC in Figure 6 are 550 mV, 38.0 mAcm^{-2}, and 0.36 respectively. These values give a solar cell efficiency of ~7.39%.

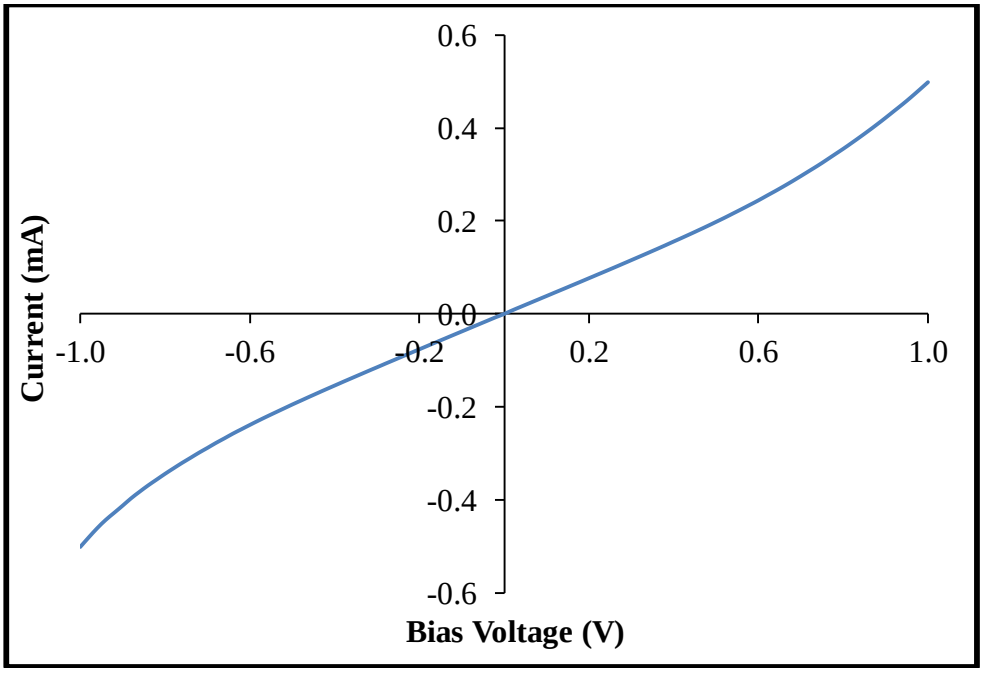

Figure 4: Linear – linear I – V characteristics of n – n – p homo – heterojunction solar cell measured under dark condition.

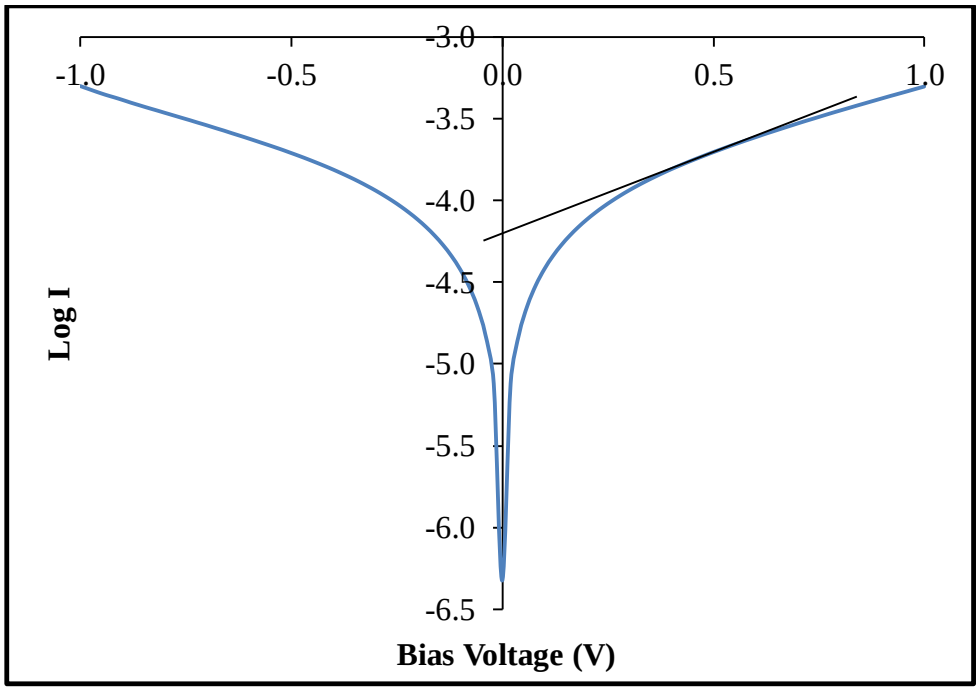

Figure 5: Log – linear I – V characteristics of n – n – p homo – heterojunction solar cell measured under dark condition.

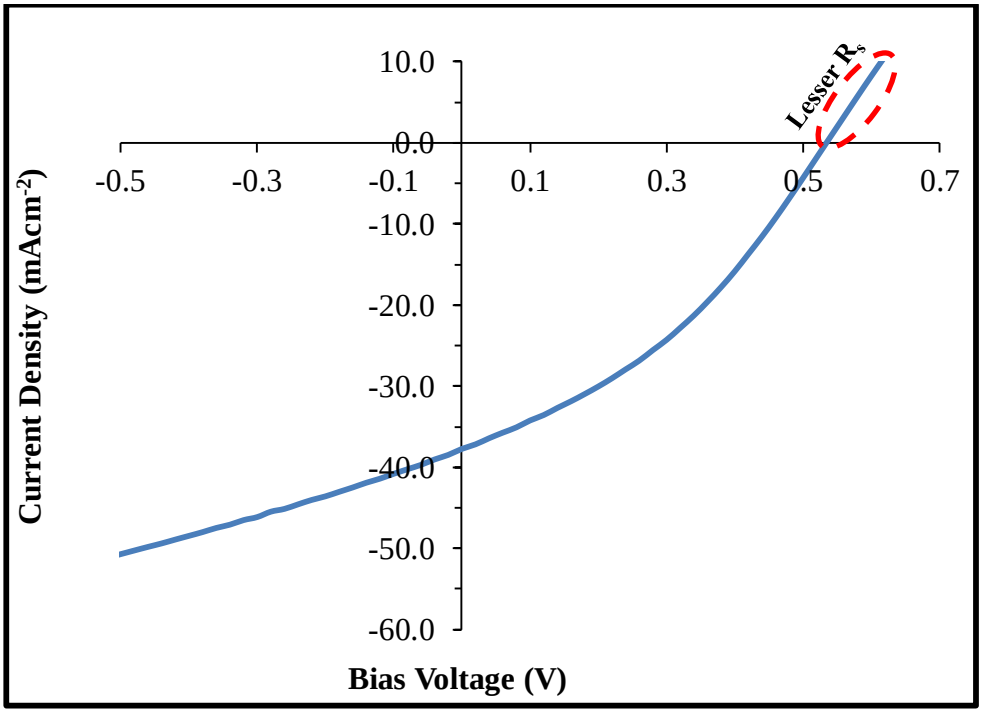

Figure 6: J – V characteristics of n – n – p homo – heterojunction solar cell measured under illumination condition.

Table 1. Obtained solar cell parameters under dark and illumination conditions for n – n Schottky barrier solar cells and n – n – p homo – heterojunction solar cells.

Device Configuration	Solar Cell Parameters Measured under Dark Condition						Solar Cell Parameters Measured under AM1.5 Illumination Condition					
	R_s (kΩ)	R_{sh} (kΩ)	n	RF	I_o (nA)	ϕ_b (eV)	R_s (kΩ)	R_{sh} (kΩ)	V_{oc} (V)	J_{sc} mAcm^{-2}	FF	η (%)
n – n Schottky Barrier Solar Cells	9.04	454.54	3.11	30.20	19.95	0.729	2.55	5.16	0.52	27.0	0.35	4.91
n – n – p Homo – heterojunction Solar Cells	1.43	1.21	3.85	1.05	39810	0.53	0.37	1.38	0.55	38.0	0.36	7.39

3.3. Comparative Study

The summary of solar cell parameters under dark and illumination conditions is given in Table 1. A good solar cell should have low R_s and large R_{sh} value. Solar cell parameters are expected to increase with low R_s value and large R_{sh} value. As seen in Table 1, SBSC has higher R_s value than the HHSC, while the R_{sh} value of SBSC is higher than that of HHSC. Nonetheless, because of the extremely high R_s value of SBSC under illumination, the effect of its large shunt resistance was not obvious on the solar cell efficiency. Thus, the low R_s value of the HHSC under illumination accounts for the improved efficiency in the solar cell.

Generally, FF is improved by large shunt resistance provided the R_s is low. Due to the large shunt resistance in SBSC, the FF is expected to be higher in SBSC. However, this was not the case because of the high R_s value in SBSC. As previously explained, this high R_s value originates from the back-contact resistance between the metal and semiconductor. The FF values obtained for both SBSC and HHSC are 0.35 and 0.36, which are comparable.

In a similar manner, J_{sc} is improved when the R_s is low and R_{sh} is large. But when the R_s is large as seen in the SBSC reported in this work, it can lead to a reduction in the J_{sc} value (Green, 1977; Singh & Ravindra, 2011). The low R_s obtained in the HHSC is a distinguished factor which enhances the J_{sc} value when compared to SBSC. Higher V_{oc} of 0.55 V was obtained in HHSC as compared to 0.52 V obtained in SBSC. This is due to the effect of p-type CdTe plated on n-CdTe. The p – type material has the potential to pin the Fermi level close to valence band; by so doing, this will increase the open circuit voltage.

4. Conclusion

Solar cells have been successfully fabricated using the Schottky barrier and homo – heterojunction device architecture. The current – voltage measurements were recorded for both solar cells under dark and illumination conditions. The Schottky barrier solar cells measured under dark condition displayed a good Schottky diode behaviour with a turn on voltage of ~0.3 V and rectification factor of ~30.20 while the homo – heterojunction solar cell displayed a poor rectifying behaviour of non – linear response having a turn on voltage of 0.0 V and poor rectification factor of ~1.05. The higher series resistance associated with Schottky barrier devices limit the solar cell efficiency of Schottky barrier solar cell. The experimental investigation revealed that Schottky barrier solar cell has high R_s value of ~2.6 kΩ while homo – heterojunction solar cell has lower R_s value of ~0.37 kΩ when measured under illumination. The low R_s seen in homo – heterojunction solar cell when compared with the Schottky barrier solar cell leads to efficiency enhancement of the homo – heterojunction solar cell. Efficiencies of ~4.91 and ~7.39 were calculated for the Schottky barrier and homo – heterojunction – based solar cells respectively. The experimental results revealed that the deposition of p-CdTe layer on glass/FTO/n – CdS/n – CdTe/ Schottky structure changes the entire electronic properties of the n – n – p homo – heterojunction solar cells and enhances the cell efficiency. Work is on-going to improve the solar cells efficiency by ensuring effective optimisation of the semiconductor materials used in the device fabrication.

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